**D Flip-flop**

* D flip-flop is the most important flip-flop in digital circuit. D flip-flop is also known as delay type flip-flop because output of D flip-flop is 1 clock pulse delay of the input applied to the D flip-flop.
* The truth table of positive edge triggered D flip-flop is given below. When there is negative edge trigger clock, it stores the previous input applied to the flip-flop. In positive edge trigger of clock, input of the d flip-flop is stored.

**D flip-flop Truth Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **Clock Edge** | **D** | **Q** | **Description** |
| ↓ | X | Q | No Change (Store previous input) |
| ↑ | 1 | 1 | Set Q to 1 |
| ↑ | 0 | 0 | Reset Q to 0 |

**Verilog Code of D flip-flop**

1. **D flip-flop without reset**

module dff(clk,d,q);

input clk,d;

output reg q;

**always @** (posedge clk)begin

q <= d;

end

endmodule

1. **D flip-flop with synchronous reset**

module dff(clk,reset,d,q);

input clk,reset,d;

output reg q;

**always @** (posedge clk)begin

if(reset)

q <= 0;

else

q <= d;

end

endmodule

1. **D flip-flop with asynchronous reset low level**

module dff(clk,reset,d,q);

input clk,reset,d;

output reg q;

**always @** (posedge clk or negedge reset)begin

if(~reset)

q <= 0;

else

q <= d;

end

endmodule

1. **D flip-flop with asynchronous reset high level**

module dff(clk,reset,d,q);

input clk,reset,d;

output reg q;

**always @** (posedge clk or posedge reset)begin

if(reset)

q <= 0;

else

q <= d;

end

endmodule